IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application		)	PATENT APPLICATION
Inventor:	Jian Chen	)	Art Unit: 2824
Application No.:	10/765,963	)	Examiner: Tran, Andrew Q.
Filed Date:	January 26, 2004	)	Customer No.: 28554
Title: METHOD OF READING NAND MEMORY TO COMPENSATE FOR COUPLING BETWEEN STORAGE ELEMENTS		)	

DECLARATION OF JIAN CHEN
PURSUANT TO 37 C.F.R. §1.131

I, JIAN CHEN, declare that:

1. I am an inventor of the invention described and claimed in the above-identified patent application. I am currently the employed by SanDisk Corporation, assignee of the present application. I have reviewed the pending application as stated in my Declaration for Patent Application and the pending claims as set forth in the RESPONSE A TO OFFICE ACTION ("RESPONSE A") accompanying this DECLARATION. I have also reviewed U.S. Patent No. 6,999,344 having a filing date if Mar. 11, 2005, and claiming priority to United States Application Ser. No. 10/601,006, filed Jun. 20, 2003, and Japanese Application Ser. No. 2003-117333, filed Apr. 22, 2003.

2. I understand that this Declaration will be filed in the United States Patent and Trademark Office in order to provide factual evidence showing that the invention claimed in the present application was completed prior to the date of Apr. 22, 2003.

3. The facts set forth hereinafter to establish that the claimed invention was completed prior to Apr. 22, 2003 all relate to acts which occurred and were carried out within the United States.

4. In early April, 2003, I was employed by SanDisk at its then Sunnyvale, California facility. On or about February 12, 2003, I conceived of the claimed invention during my work at SanDisk. On or about April, 14, 2003, I memorialized my conception in the invention disclosure attached hereto as Exhibit 1, the invention disclosure having a creation date of April 14, 2003.

5. Subsequent to filing the disclosure, on information and belief, the disclosure was forwarded to the attorney of record in this application for preparation. Between about May 2003 and January 2004, I worked diligently with the attorney of record to prepare and file the instant application.

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6. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 3/27/2007 (Japan Time)

By: _____
Jian Chen

EXHIBIT 1

Invention Disclosure Form
Privileged & Confidential

SanDisk

Rev 3.1 (4/11/03)

Date:	April 14, 2003	**Dept#/Name:**	230
Name of Originator:	Jian Chen	**Supervisor:**	George Samachisa
Project/Product:	MLC NAND		
Inventor(s):	Jian Chen		
Title of Invention:	Method of Reading (NAND) Flash Memory with reduced Adjacent Cell Coupling		

Problem Addressed by Invention:

WL2WL Coupling is getting worse esp. for 90nm, 70nm and beyond. Very difficult to shield with process method.

Previous Approaches to Solving Problem:

No good method so far. We are affected with slower performance, less reliability, and more complex process.

Brief Description of Invention: (Attach all relevant drawings, specs, flowcharts, design review or notebook entries)

See attached file. Basic Points: a) To compensate for the WL2WL Yupin effect by reading the next WL data. b.) The next WL data is used to adjust the sense point of the previous WL read, thus read the previous WL Vt with shifted value, thus to obtain pre-Yupin value.

Approximate Date of Conception	Feb 12, 2003
Additional Future Features and/or Applications:	
Is this invention going into a product? If so, when will the product be offered for sale?	2003?
Will the invention be described in a publication? If so, when?	
Joint Development project with a non-SanDisk party? If so, who?	Yes/Toshiba

Signatures:

Originator: Jian Chen	**Read & Understood by:**
Supervisor:	**Comments:**

Additional Comments: see attached

Method of Reading (NAND) Flash Memory with reduced Adjacent Cell Coupling

1. Background: Basic Problem

This is for a by now well documented problem: for MLC flash memory, the adjacent cell coupling (Yupin) effect. Specifically as MLC NAND scales further to 90nm, 70nm and beyond, it is expected that the WL2WL Yupin will get much worse due to ever much closer. This same trend is also expected to other types of NVM devices, such as NOR type Flash memory devices. For example, it is expected (some measurements, some simulation) that the WL2WL Yupin effect is about 0.2V for 90nm, and 0.3V for 70nm generation of MLC NAND.

The BL2BL Yupin coupling is countered by PassWrite or DeepSlit process. So far no effective countermeasure have been found to counter the ever larger WL2WL coupling.

This disclosure is try to propose a new read method to reduce the effect of WL2WL Yupin effect for MLC NAND memory, and the same principle also applied to other types of NVM memories as well.

2. Basic Idea

The basic idea is: to do iterative read to compensate for the WL2WL Yupin coupling. For example, to read a page on WLn, first do a rough read of WLn+1. This is shown in Figure 1 below. Before the WLn page read, we do a "rough" WLn+1 read at V_check point, which is estimated to be the mid-point of the whole Vt distribution. In the Vt setting example below, it happened to be the Vcg00r value we are currently using. In future this value may change, and V_check should be an independent parameter with separate set of DAC table.

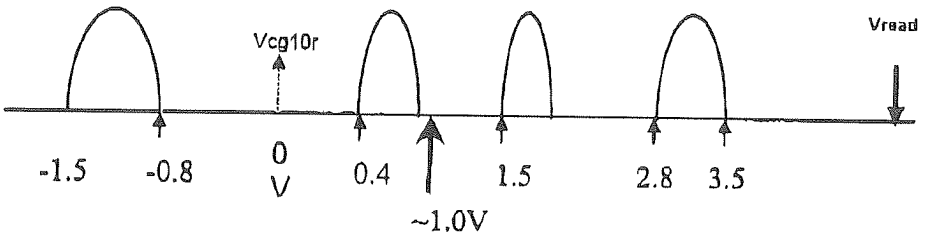

Fig.1 Next WL movement detection read. To detect the whole Vt window mid-point. For "1"s, the amount of Yupin movement is ignored, for "0"s, the Yupin movement is compensated. As a whole the total WL2WL Yupin widening is cut by half.

When WLn+1 is read with V_check, we will know if the bits are above Vt of V_check or below of V_check. This also means we would know if the previous wordline WLn cells have been WL2WL Yupin shift amount. Take 70nm generation for example, we know if the WLn+1 cells are above V_check, then the WLn cell have been shifted up between 0.15V to 0.3V. And for cells that are next to WLn+1 cell which are below V_check, the amount of WL2WL shift is between 0V to 0.15V.

The second part of the basic idea is: armed with that knowledge, we can do WLn read as bitline dependent. That is, we can adjust the bitline direction at WLn read, to compensate the amount of shift it has experienced. This is illustrate in Figure 2. The exact method of the shifted sensing method and data are described in the following sections.

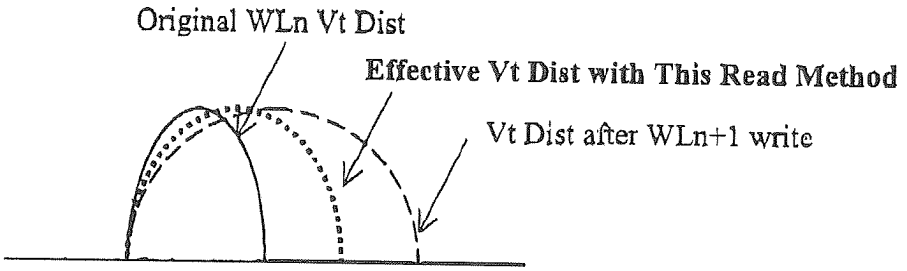

Fig.2 The effect of new compensation reading method.

The tradeoff here is that it would require two WL reads to finish one page read. For the case of NAND MLC, since lower page read requires two reads, this will add one more read, so the total read speed increase is one more read, or 50%.

Of course this principle can be applied to cut the WL2WL Yupin effect by n times, if we do many V_check_n, and break the Vt dist window to n parts.

3. Some Data and Adjusted Sensing Method

One of the key to realize the above concept is the method to do the adjusted sensing. This means to use the data obtained from WLn+1 read, to adjust the WLn read. For MLC NAND, there are several methods.

One such method is to use the WLn+1 data, to adjust the Vsen and Vclamp voltage during the sensing. This means, we are sensing certain bits with shifted Vt. In other words, when if a cell has Vt of 0.5V. Due to Yupin effect of next WL, it is shifted to 0.8V. Regular reading would have results in reading of 0.8V. But since we change the sensing point during read, and automatically substrate 0.15V from it, so we will end up with 0.5+0.15=0.65V.

Figures 3-5 are data taken showing Vt dist. shifted with shifted Vsen and Vclamp. This is for the current sense circuit used in current product.

This method can also be applied with the new ABL sensing method, which we use two different value capacitors for the sensing.

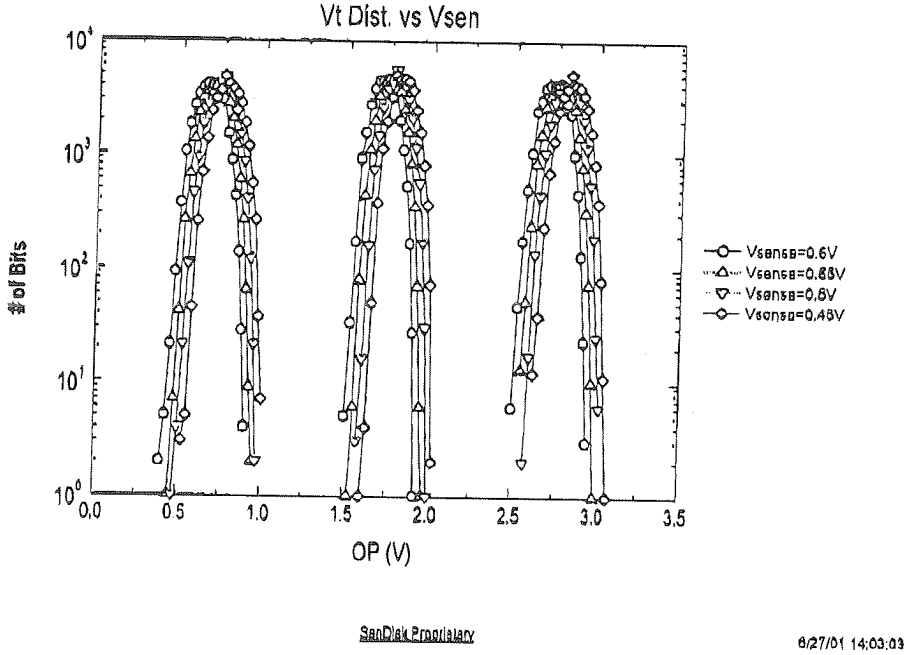

Figure 3 Measured Vt dist as a function of Vsen.

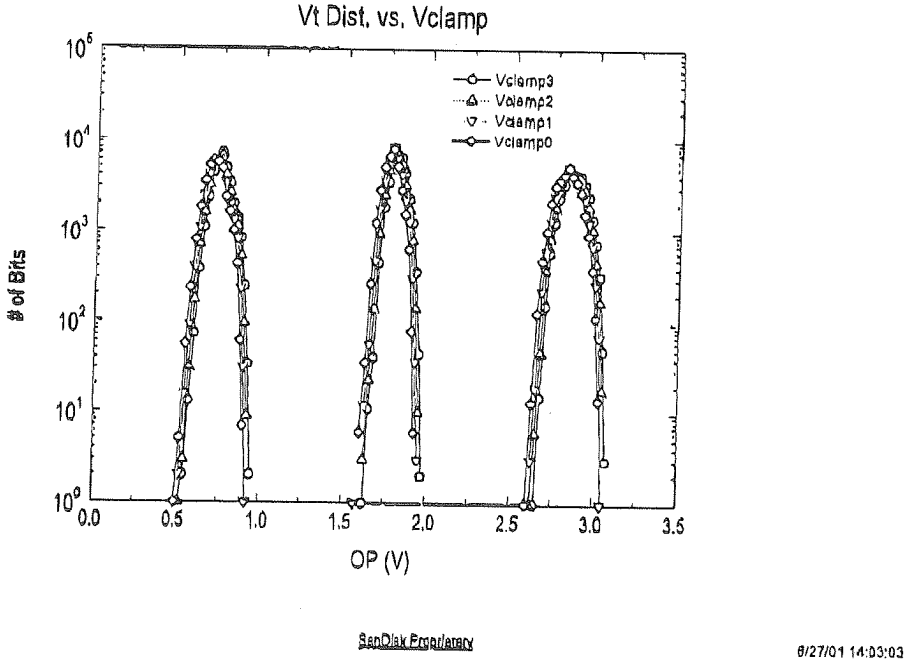

Figure 4 Measured Vt dist as a function of Vclamp.

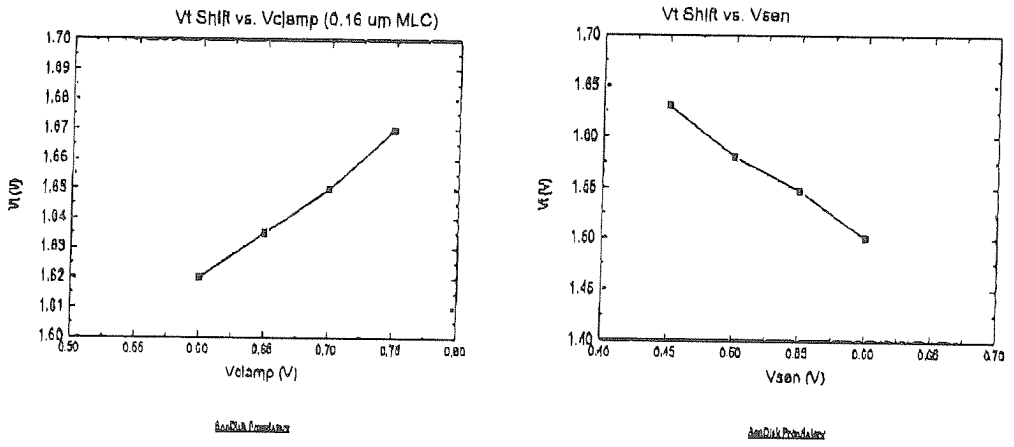

Figure 5 Measured Vt dist as a function of Vsen and Vclamp